

YTY UNiCORE

Memory Module Data Sheet

DDR4-2666(CL19) 288-Pin

U-DIMM 8GB

**Based on 8Gb UniCORE Die
(1024M x 64-bit)**

Version 1-0

Revision History

Version	Changes	Page	Date
V1-0	Formal release	-	2020/07/08

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General Description :

GD4UD26N08C4U000 is DDR4-2666(CL19)-19-19 SDRAM memory module. The SPD is programmed to JEDEC standard latency 2666Mbps timing of 19-19-19 at 1.2V. The module is composed of 8Gb CMOS DDR4 SDRAMs in FBGA package and one 4Kbit EEPROM in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features :

- Power supply (Normal)
 - VDD & VDDQ = 1.2V +5% / -5%
 - VPP = 2.5V +10% / -5%
 - VDDSPD = 2.5V (2.25V to 3.6V)
- Burst Length (BL):8 and 4 with Burst Chop(BC)
- Bi-directional, differential data strobe (DQS and /DQS)
- Differential clock input operation
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture; two data transfers per clock cycle
- 16 internal banks; 4 groups of 4 banks each
- Internal self calibration through ZQ pin (RZQ:240 ohm±1%)
- Low-power auto refresh (LPASR)
- Tc of 0°C to 95°C
 - 64ms, 8192-cycle refresh at 0°C to 85°C
 - 32ms, 8192-cycle refresh at 85°C to 95°C
- 8-bit pre-fetch architecture
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals.
- Data bus inversion for data bus(DBI)
- Data bus Write CRC
- Lead-free and Halogen-free products are RoHS Compliant

Pin Assignment :

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	12V	41	NC	81	BA0	121	DM6,DBI6	161	DQ9	201	CB3	241	VSS	281	VSS
2	VSS	42	VSS	82	RAS_n/A16	122	NC	162	VSS	202	VSS	242	DQ33	282	DQ59
3	DQ4	43	DQ30	83	VDD	123	VSS	163	DQS1_C	203	CKE1	243	VSS	283	VSS
4	VSS	44	VSS	84	CS0_n	124	DQ54	164	DQS1_T	204	VDD	244	DQS4_C	284	VDDSPD
5	DQ0	45	DQ26	85	VDD	125	VSS	165	VSS	205	RFU	245	DQS4_T	285	SDA
6	VSS	46	VSS	86	CAS_n/A15	126	DQ50	166	DQ15	206	VDD	246	VSS	286	VPP
7	DM0,DBI0	47	CB4	87	ODT0	127	VSS	167	VSS	207	BG1	247	DQ39	287	VPP
8	NC	48	VSS	88	VDD	128	DQ60	168	DQ11	208	ALERT_n	248	VSS	288	VPP
9	VSS	49	CB0	89	CS1_n	129	VSS	169	VSS	209	VDD	249	DQ35		
10	QD6	50	VSS	90	VDD	130	DQ56	170	DQ21	210	A11	250	VSS		
11	VSS	51	DM8,DBI8	91	ODT1	131	VSS	171	VSS	211	A7	251	DQ45		
12	DQ2	52	NC	92	VDD	132	DM7,DBI7	172	DQ17	212	VDD	252	VSS		
13	VSS	53	VSS	93	NC	133	NC	173	VSS	213	A5	253	DQ41		
14	DQ12	54	CB6	94	VSS	134	VSS	174	DQS2_C	214	A4	254	VSS		
15	VSS	55	VSS	95	DQ36	135	DQ62	175	DQS2_T	215	VDD	255	DQS5_C		
16	DQ8	56	CB2	96	VSS	136	VSS	176	VSS	216	A2	256	DQS5_T		
17	VSS	57	VSS	97	DQ32	137	DQ58	177	DQ23	217	VDD	257	VSS		
18	DM1,DBI1	58	RESET_n	98	VSS	138	VSS	178	VSS	218	CK1_T	258	DQ47		
19	NC	59	VDD	99	DM4,DBI4	139	SA0	179	DQ19	219	CK1_C	259	VSS		
20	VSS	60	CKE0	100	NC	140	SA1	180	VSS	220	VDD	260	DQ43		
21	DQ14	61	VDD	101	VSS	141	SCL	181	DQ29	221	VTT	261	VSS		
22	VSS	62	ACT_n	102	DQ38	142	VPP	182	VSS	222	PARITY	262	DQ53		
23	DQ10	63	BG0	103	VSS	143	VPP	183	DQ25	223	VDD	263	VSS		
24	VSS	64	VDD	104	DQ34	144	RFU	184	VSS	224	BA1	264	DQ49		
25	DQ20	65	A12/BC_n	105	VSS	145	12V	185	DQS3_C	225	A10/AP	265	VSS		
26	VSS	66	A9	106	DQ44	146	VREFCA	186	DQS3_T	226	VDD	266	DQS6_C		
27	DQ16	67	VDD	107	VSS	147	VSS	187	VSS	227	RFU	267	DQS6_T		
28	VSS	68	A8	108	DQ40	148	DQ5	188	DQ31	228	WE_n/A14	268	VSS		
29	DM2,DBI2	69	A6	109	VSS	149	VSS	189	VSS	229	VDD	269	DQ55		
30	NC	70	VDD	110	DM5,DBI5	150	DQ1	190	DQ27	230	NC	270	VSS		
31	VSS	71	A3	111	NC	151	VSS	191	VSS	231	VDD	271	DQ51		
32	DQ22	72	A1	112	VSS	152	DQS0_C	192	CB5	232	A13	272	VSS		
33	VSS	73	VDD	113	DQ46	153	DQS0_T	193	VSS	233	VDD	273	DQ61		
34	DQ18	74	CK0_t	114	VSS	154	VSS	194	CB1	234	NC	274	VSS		
35	VSS	75	CK0_c	115	DQ42	155	DQ7	195	VSS	235	NC	275	DQ57		
36	DQ28	76	VDD	116	VSS	156	VSS	196	DQS8_C	236	VDD	276	VSS		
37	VSS	77	VTT	117	DQ52	157	DQ3	197	DQS8_T	237	NC	277	DQS7_C		
38	DQ24	78	EVENT_n	118	VSS	158	VSS	198	VSS	238	SA2	278	DQS7_T		
39	VSS	79	A0	119	DQ48	159	DQ13	199	CB7	239	VSS	279	VSS		
40	DM3,DBI3	80	VDD	120	VSS	160	VSS	200	VSS	240	DQ37	280	DQ63		

Pin Description :

Pin Name	Description	Pin Name	Description
A0–A17 ¹	SDRAM address bus	SCL	I2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD-TSE
RAS_n ²	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n ³	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n ⁴	SDRAM write enable	12V	Optional power Supply on socket but not used on UDIMM [*]
CS0_n, CS1_n	DIMM Rank Select Lines	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	SDRAM on-die termination control lines	VDDSPD	Serial SPD/TSE positive power supply
ACT_n	SDRAM activate	ALERT_n	SDRAM ALERT_n
DQ0–DQ63	DIMM memory data bus	RESET_n	Set DRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS8_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS8_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
DM0_n–DM8_n, DBI0_n–DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)		
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)		
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.

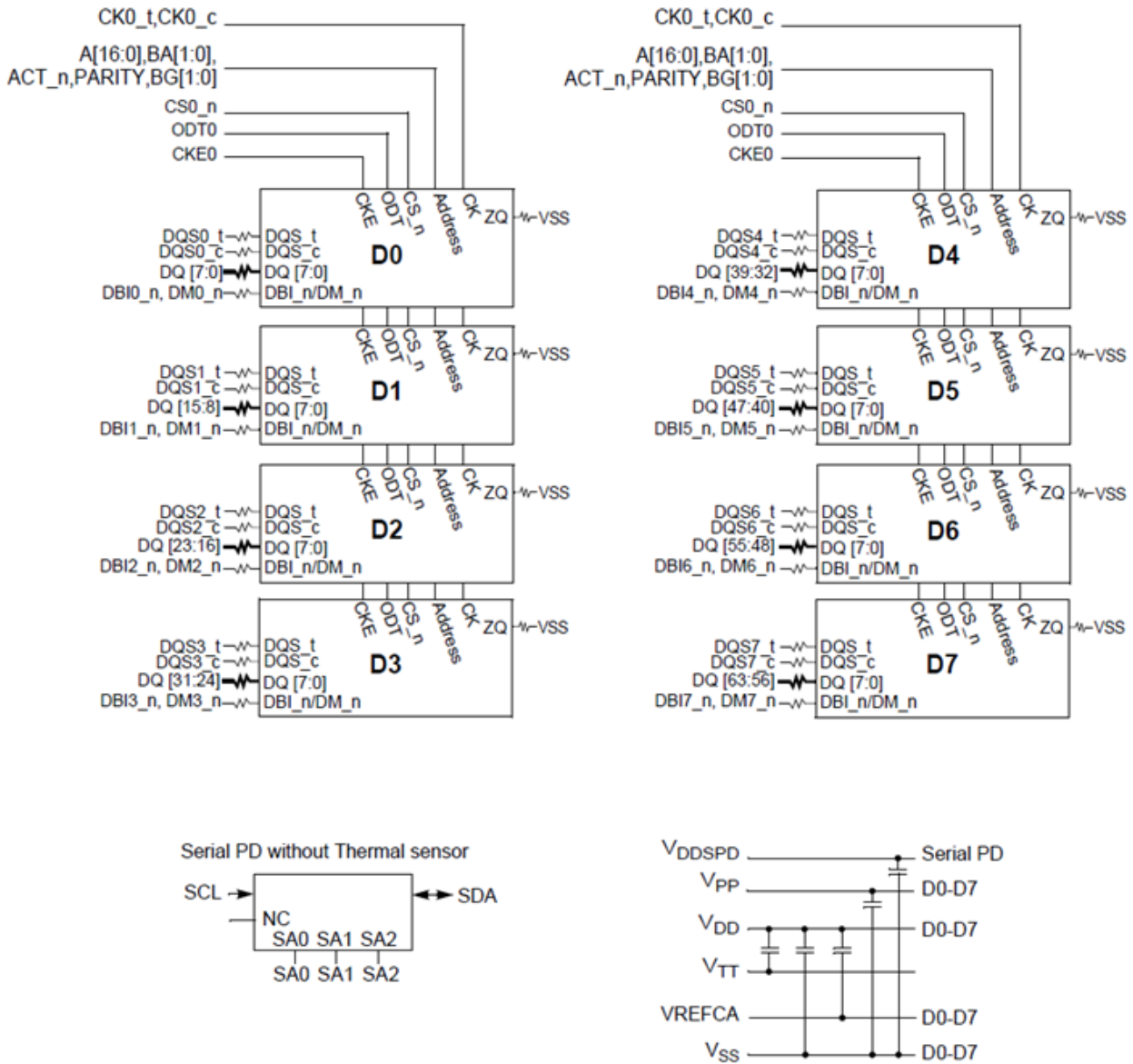
2. RAS_n is a multiplexed function with A16.

3. CAS_n is a multiplexed function with A15.

4. WE_n is a multiplexed function with A14.

Block Diagram :

[8GB – 1Rank, 1024Mx8 DDR4 SDRAMs]



Note 1: CK1_t, CK1_c terminated with $75\Omega \pm 5\%$ resistor...

Note 2: Unless otherwise noted resistors are $15\Omega \pm 5\%$...

Note 3: ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram...

Absolute Maximum Ratings :

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.5	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~1.5	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~3.0	V
Voltage on any pin relative to Vss	VIN, Vout	-0.3 ~ 1.5	V
Storage temperature	TSTG	-55 ~ +100	°C

Note: DDR4 SDRAM component specification.

Operation Temperature Condition :

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	°C	
Extended Temperature Range (Optional)	TC	+85~+95	°C	1

Note: (1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 3.9μs

DC Operating Condition:

Voltage referenced to Vss = 0V, VDD&VDDQ=1.2V±0.06V, Tc = 0 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.14	1.2	1.26	V	1,2,3
	VDDSPD	2.25	2.5	3.6	V	
Supply Voltage for Output	VDDQ	1.14	1.2	1.26	V	1,2,3
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3
Reference Voltage for CMD/ADD	VREFCA, (DC)	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	4
Termination Voltage	VTT	0.49 x VDDQ-20mV	0.5 x VDD	0.51 x VDDQ+20mV	V	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.

(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

(3) The DC bandwidth is limited to 20MHz.

(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

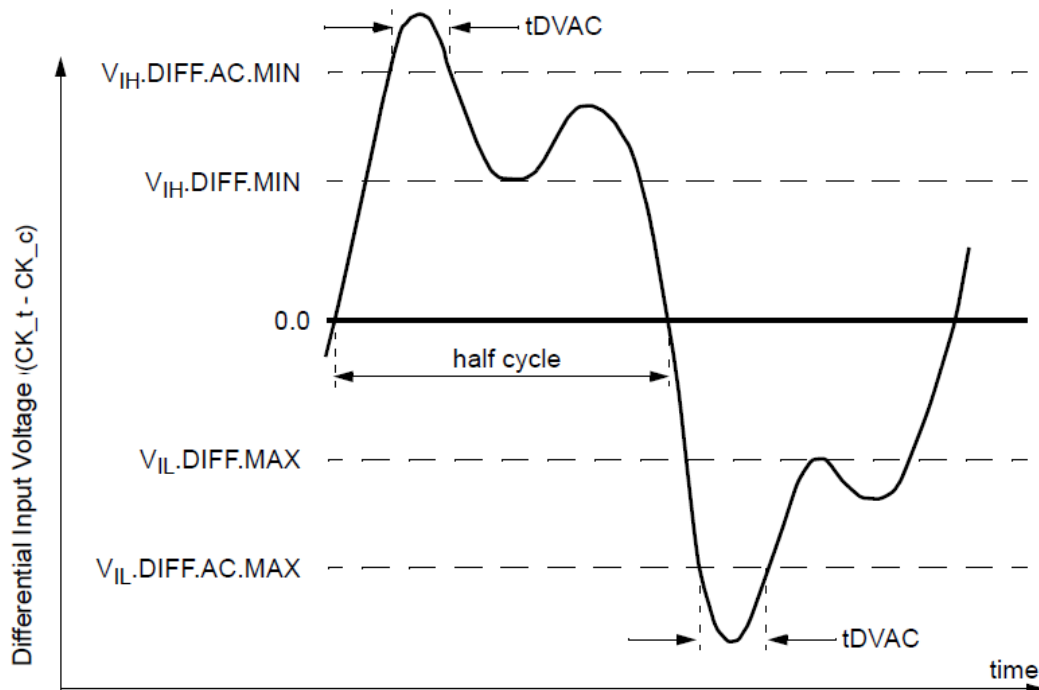
Input DC & AC Logic Level for single-ended signals :

Parameter	Symbol	DDR4-2400		DDR4-2666/3200		Unit	Note
		Min	Max	Min	Max		
DC Input logic high voltage	VIH (DC)	VREF+75	VDD	VREF+65	VDD	mV	1
DC Input logic low voltage	VIL (DC)	VSS	VREF-75	VSS	VREF-65	mV	1
AC input logic high	VIH(AC)	VREF+100	Note 2	VREF+90	Note 2	mV	1
AC input logic low	VIL(AC)	Note 2	VREF-100	Note 2	VREF-90	mV	1

Note: 1. See "Overshoot and Undershoot Specifications" on section.

2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than $\pm 1\%$ VDD (for reference : approx. $\pm 12\text{mV}$)

Input AC & DC Logic Level for Differential signals :



Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Note
		Min	Min	Min	Max	Min	Max		
Differential input high	VIHdiff	0.135	Note 3	0.135	Note 3	0.11	Note 3	V	1
Differential input low	VILdiff	Note 3	-0.135	Note 3	-0.135	Note 3	-0.11	V	1
Differential input high AC	VIHdiff (AC)	2x(VIH(ac)-Vref)	Note 3	2x(VIH(ac)-Vref)	Note 3	2x(VIH(ac)-Vref)	Note 3	V	2
Differential input low AC	VILdiff (AC)	Note 3	2x(VIL(ac)-Vref)	Note 3	2x(VIL(ac)-Vref)	Note 3	2x(VIL(ac)-Vref)	V	2

Notes:

- (1) Used to define a differential signal slew-rate.
- (2) For CK_t – CK_c use VIH/VIL(ac) of ADD/CMD and VREFCA
- (3) These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot on Component Datasheet.

IDD Specification :

VDDQ = VDD = 1.2V(1.14V~1.26V)

Symbol	Condition	8GB	Unit
IDD0 ¹	One bank ACTIVATE-PRECHARGE current	224	mA
IPP0 ¹	One bank ACTIVATE-PRECHARGE,wordline boost,IPP current	32	mA
IDD1 ¹	One Bank Active-Read-Precharge Current	256	mA
IDD2N ²	Precharge Standby Current	144	mA
IDD2NT ¹	Precharge standby ODT current	168	mA
IDD2P ²	Precharge Power-Down Current	88	mA
IDD2Q ²	Precharge Quiet Standby Current	136	mA
IDD3N ²	Active standby current	216	mA
IPP3N ²	Active standby IPP current	32	mA
IDD3P ²	Active Power-Down Current	152	mA
IDD4R ¹	Burst Read Current	792	mA
IDD4W ¹	Burst write current	736	mA
IDD5B ¹	Burst refresh current (1x REF)	1480	mA
IPP5B ¹	Burst refresh IPP current (1x REF)	144	mA
IDD6N ²	Self refresh current: Normal temperature range (0–85°C)	168	mA
IDD6E ²	Self refresh current: Extended temperature range (0–95°C)	272	mA
IDD7 ¹	Bank interleave read current	1176	mA
IPP7 ¹	Bank interleave read IPP current	88	mA
IDD8 ²	Maximum power-down current	176	mA

Note:

1. One module rank in the active IDD/PP, the other rank in IDD2N/PP2N.
2. All ranks in this IDD/PP condition.
3. IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

Timings used for IDD, IPP and IDDQ Measurement :

Symbol		DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Units
Bin(CL-tRCD-tRP)		13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
Parameter		Min	Min	Min	Min	Min	Min	
tCK		1.071	0.937	0.833	0.75	0.682	0.625	ns
CL		13	15	17	19	21	22	nCK
CWL		12	14	16	18	20	20	nCK
nRCD		13	15	17	19	21	22	nCK
nRC		45	51	56	62	68	74	nCK
nRAS		32	36	39	43	47	52	nCK
nRP		13	15	17	19	21	22	nCK
nFAW	X4	16	16	16	16	16	16	nCK
	X8	23	26	28	31	34	34	nCK
	X16	32	36	40	44	48	48	nCK
nRRDS	X4	4	4	4	4	4	4	nCK
	X8	4	4	4	4	4	4	nCK
	X16	6	7	8	8	9	9	nCK
nRRDL	X4	6	6	7	8	8	8	nCK
	X8	6	6	7	8	8	8	nCK
	X16	7	8	9	10	11	11	nCK
tCCD_S		4	4	4	4	4	4	nCK
tCCD_L		5	6	6	7	8	8	nCK
tWTR_S		3	3	3	4	4	4	nCK
tWTR_L		7	8	9	10	11	12	nCK
nRFC 2Gb		150	171	193	214	235	256	nCK
nRFC 4Gb		243	278	313	347	382	416	nCK
nRFC 8Gb		327	374	421	467	514	560	nCK
nRFC 16Gb		514	587	661	734	807	880	nCK

Timing Parameters:

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Clock Timing										
Clock period average(DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns		
Clock period average	tCK (AVG) (DLL_ON)	0.83	<0.937	0.75	<0.833	0.63	<0.682	ns	14	
High pulse width average	tCH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(AVG)		
Low pulse width average	tCL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(AVG)		
Clock period jitter	Total	tJITper_tot	-42	42	-38	38	-32	32	ps	18 ,19
	Deterministic	tJITper_dj	-21	21	-19	19	-16	16	ps	18
	DLL locking	tJITper,lck	-33	33	-30	30	-25	25	ps	
Clock absolute period	tCK (ABS)	MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK (AVG) MAX + tJITper_tot MAX						ps		
Clock absolute high pulse width (includes duty cycle jitter)	tCH (ABS)	0.45	-	0.45	-	0.45	-	tCK(AVG)		
Clock absolute low pulse width (includes duty cycle jitter)	tCL (ABS)	0.45	-	0.45	-	0.45	-	tCK(AVG)		
Cycle-to-cycle jitter	Total	tJITcc_tot	-	83	-	75	-	62	ps	
	DLL locking	tJITcc,lck	-	67	-	60	-	50	ps	
Cumulative error across	2 cycles	tERR2per	-61	61	-55	55	-46	46	ps	
	3 cycles	tERR3per	-73	73	-66	66	-55	55	ps	
	4 cycles	tERR4per	-81	81	-73	73	-61	61	ps	
	5 cycles	tERR5per	-87	87	-78	78	-65	65	ps	
	6 cycles	tERR6per	-92	92	-83	83	-69	69	ps	
	7 cycles	tERR7per	-97	97	-87	87	-73	73	ps	
	8 cycles	tERR8per	-101	101	-91	91	-76	76	ps	
	9 cycles	tERR9per	-104	104	-94	94	-78	78	ps	
	10 cycles	tERR10per	-107	107	-96	96	-80	80	ps	
	11 cycles	tERR11per	-110	110	-99	99	-83	83	ps	
	12 cycles	tERR12per	-112	112	-101	101	-84	84	ps	
n=13,14...49, 50cycles	tERRnper	tERRnper MIN = (1 + 0.68ln[n]) × tJITper_tot MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper_tot MAX						ps		

Parameter		Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
DQ Input Timing										
Data setup time to DQS_t, DQS_c	Base(calibrated V _{REF})	tDS	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.28tCK)					-		
	Noncalibrated V _{REF}	tPDA_S	minimum of 0.5UI					UI	23	
Data hold time from DQS_t, DQS_c	Base(calibrated V _{REF})	tDS	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.28tCK)					-		
	Noncalibrated V _{REF}	tPDA_S	minimum of 0.5UI					UI	23	
DQ and DM minimum data pulse width for each input		tDIPW	0.58	-	0.58	-	0.58	-	UI	
DQ Output Timing (DLL enabled)										
DQS_t, DQS_c to DQ skew, per group, per access		tDQSQ	-	0.17	-	0.18	-	0.20	UI	
DQ output hold time from DQS_t, DQS_c		tQH	0.74	-	0.74	-	0.70	-	UI	
Data Valid Window per device: tQH -tDQSQ each device's output per UI		tDVWd	0.64	-	0.64	-	0.64	-	UI	
Data Valid Window per device, per pin: tQH - tDQSQ each device's output per UI		tDVWp	0.72	-	0.72	-	0.72	-	UI	
DQ Low-Z time from CK_t, CK_c		tLZDQ	-330	175	-310	170	-250	160	ps	
DQ High-Z time from CK_t, K_c		tHZDQ	-	175	-	170	-	160	ps	
DQ Strobe Input Timing										
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1tCKpreamble		tDQSS _{1ck}	-0.27	0.27	-0.27	0.27	-0.27	0.27	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2tCKpreamble		tDQSS _{2ck}	-0.50	0.50	-0.50	0.50	-0.50	0.50	CK	
DQS_t, DQS_c differential input low pulse width		tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	CK	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQ Strobe Input Timing									
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge	tDSS	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge	tDSH	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c differential WRITE preamble for 1 ^t CKpreamble	tWPRE _{1ck}	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential WRITE preamble for 2 ^t CKpreamble	tWPRE _{2ck}	1.8	–	1.8	–	1.8	–	CK	
DQS_t, DQS_c differential WRITE postamble	tWPST	0.33	–	0.33	–	0.33	–	CK	
DQS Strobe Output Timing (DLL enabled)									
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	tDQSCK	–175	175	–170	170	–160	160	ps	
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKi	–	290	–	270	–	260	ps	
DQS_t, DQS_c differential output high time	tQSH	0.4	–	0.4	–	0.4	–	CK	
DQS_t, DQS_c differential output low time	tQSL	0.4	–	0.4	–	0.4	–	CK	
DQS_t, DQS_c Low-Z time (RL - 1)	tLZDQS	–330	175	–310	170	–250	160	ps	
DQS_t, DQS_c High-Z time (RL + BL/2)	tHZDQS	–	175	–	170	–	160	ps	
DQS_t, DQS_c differential READ preamble for 1 ^t CKpreamble	tRPRE _{1ck}	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential READ preamble for 2 ^t CKpreamble	tRPRE _{2ck}	1.8	–	1.8	–	1.8	–	CK	
DQS_t, DQS_c differential READ postamble	tRPST	0.33	–	0.33	–	0.33	–	CK	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Command and Address Timing										
DLL locking time	tDLLK	768	–	1024	–	1024	–	CK	2, 4	
CMD, ADDR setup time to CK_t, CK_c Base referenced to V _{IH(AC)} and V _{IL(AC)} levels	Base	tIS	62	–	55	–	40	–	ps	
	V _{REFCA}	tISVREF	162	–	145	–	130	–	ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to V _{IH(DC)} and V _{IL(DC)} levels	Base	tIH	87	–	80	–	65	–	ps	
	V _{REFCA}	tIHVREF	162	–	145	–	130	–	ps	
CTRL, ADDR pulse width for each input	tIPW	410	–	385	–	340	–	ps		
ACTIVATE to internal READ or WRITE delay	tRCD	14.2	–	14.3	–	13.8	–	ns		
PRECHARGE command period	tRP	14.2	–	14.3	–	13.8	–	ns		
ACTIVATE-to-PRECHARGE command period	tRAS	32	9xtREFI	32	9xtREFI	32	9xtREFI	ns	13	
ACTIVATE-to-ACTIVATE or REF command period	tRC	46.2	–	46.3	–	45.8	–	ns	13	
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size	tRRD_S (1/2KB)	MIN = greater of 4CK or 3.3ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.5ns		CK	1	
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size	tRRD_S (1KB)	MIN = greater of 4CK or 3.3ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.5ns		CK	1	
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size	tRRD_S (2KB)	MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		CK	1	
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size	tRRD_L (1/2KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		CK	1	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Command and Address Timing										
DLL locking time	tDLLK	768	–	1024	–	1024	–	CK	2, 4	
CMD, ADDR setup time to CK_t, CK_c Base referenced to V _{IH(AC)} and V _{IL(AC)} levels	Base	tIS	62	–	55	–	40	–	ps	
	V _{REFCA}	tISVREF	162	–	145	–	130	–	ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to V _{IH(DC)} and V _{IL(DC)} levels	Base	tIH	87	–	80	–	65	–	ps	
	V _{REFCA}	tIHVREF	162	–	145	–	130	–	ps	
CTRL, ADDR pulse width for each input	tIPW	410	–	385	–	340	–	ps		
ACTIVATE to internal READ or WRITE delay	tRCD	14.2	–	14.3	–	13.8	–	ns		
PRECHARGE command period	tRP	14.2	–	14.3	–	13.8	–	ns		
ACTIVATE-to-PRECHARGE command period	tRAS	32	9xtREFI	32	9xtREFI	32	9xtREFI	ns	13	
ACTIVATE-to-ACTIVATE or REF command period	tRC	46.2	–	46.3	–	45.8	–	ns	13	
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size	tRRD_S (1/2KB)	MIN = greater of 4CK or 3.3ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.5ns		CK	1	
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size	tRRD_S (1KB)	MIN = greater of 4CK or 3.3ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 2.5ns		CK	1	
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size	tRRD_S (2KB)	MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		CK	1	
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size	tRRD_L (1/2KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		CK	1	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Command and Address Timing									
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size	tRRD_L (1KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size	tRRD_L (2KB)	MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		CK	1
Four ACTIVATE windows for 1/2KB page size	tFAW (1/2KB)	MIN = greater of 16CK or 13ns		MIN = greater of 16CK or 12ns		MIN = greater of 16CK or 10ns		ns	
Four ACTIVATE windows for 1KB page size	tFAW (1KB)	MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns		ns	
Four ACTIVATE windows for 2KB page size	tFAW (2KB)	MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		ns	
Command and Address Timing									
WRITE recovery time	tWR	MIN = 15ns						ns	5, 10, 1
	tWR2	MIN = 1CK + tWR						CK	5, 11, 1
WRITE recovery time when CRC and DM are both enabled	tWR_CRC_DM	MIN = tWR + greater of (5CK or 3.75ns)						CK	6, 10, 1
	tWR_CRC_DM2	MIN = 1CK + tWR_CRC_DM						CK	6, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group	tWTR_L	MIN = greater of 4CK or 7.5ns						CK	5, 10, 1
	tWTR_L2	MIN = 1CK + tWTR_L						CK	5, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	tWTR_L_CRC_DM	MIN = tWTR_L + greater of (5CK or 3.75ns)						CK	6, 10, 1
	tWTR_L_CRC_DM2	MIN = 1CK + tWTR_L_CRC_DM						CK	6, 11, 1

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Command and Address Timing									
Delay from start of internal WRITE transaction to internal READ command – Different bank group	tWTR_S	MIN = greater of (2CK or 2.5ns)						CK	5, 7, 8, 10, 1
	tWTR_S2	MIN = 1CK + tWTR_S						CK	5, 7, 8, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	tWTR_S_CRC_DM	MIN = tWTR_S + greater of (5CK or 3.75ns)						CK	6, 7, 8, 10, 1
	tWTR_S_CRC_DM2	MIN = 1CK + tWTR_S_CRC_DM						CK	6, 7, 8, 11, 1
READ-to-PRECHARGE time	tRTP	MIN = greater of 4CK or 7.5ns						CK	1
CAS_n-to-CAS_n command delay to different bank group	tCCD_S	4	–	4	–	4	–	CK	
CAS_n-to-CAS_n command delay to same bank group	tCCD_L	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	CK	15
Auto precharge write recovery + precharge time	tDAL (MIN)	MIN = WR + ROUNDUPtRP/tCK (AVG); MAX = N/A						CK	
MRS Command Timing									
MRS command cycle time	tMRD	8	–	8	–	8	–	CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK, 10ns)							1
MRS command cycle time in CAL mode	tMRD_CAL	MIN = tMOD + tCAL						CK	
MRS command update delay	tMOD	MIN = greater of (24nCK, 15ns)						CK	1
MRS command update delay in PDA mode	tMOD_PDA	MIN = tMOD						CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL CK						CK	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Command and Address Timing									
Delay from start of internal WRITE transaction to internal READ command – Different bank group	tWTR_S	MIN = greater of (2CK or 2.5ns)						CK	5, 7, 8, 10, 1
	tWTR_S2	MIN = 1CK + tWTR_S						CK	5, 7, 8, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	tWTR_S_CRC_DM	MIN = tWTR_S + greater of (5CK or 3.75ns)						CK	6, 7, 8, 10, 1
	tWTR_S_CRC_DM2	MIN = 1CK + tWTR_S_CRC_DM						CK	6, 7, 8, 11, 1
READ-to-PRECHARGE time	tRTP	MIN = greater of 4CK or 7.5ns						CK	1
CAS _n -to-CAS _n command delay to different bank group	tCCD_S	4	–	4	–	4	–	CK	
CAS _n -to-CAS _n command delay to same bank group	tCCD_L	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	CK	15
Auto precharge write recovery + precharge time	tDAL (MIN)	MIN = WR + ROUNDUP(tRP/tCK (AVG)); MAX = N/A						CK	
MRS Command Timing									
MRS command cycle time	tMRD	8	–	8	–	8	–	CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK, 10ns)							1
MRS command cycle time in CAL mode	tMRD_CAL	MIN = tMOD + tCAL						CK	
MRS command update delay	tMOD	MIN = greater of (24nCK, 15ns)						CK	1
MRS command update delay in PDA mode	tMOD_PDA	MIN = tMOD						CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL CK						CK	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
MRS Command Timing									
MRS command to DQS drive in preamble training	tSDO	MIN = tMOD + 9ns						CK	
MPR Command Timing									
Multipurpose register recovery time	tMPRR	MIN = 1CK						CK	
Multipurpose register write recovery time	tWR_MPRR	MIN = tMOD + AL + PL							
CRC Error Reporting Timing									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10	CK	
CA Parity Timing									
Parity latency	PL	5	–	5	–	6	–	CK	
Commands uncertain to be executed during this time	tPAR_UNKNOWN	–	PL	–	PL	–	PL	CK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	–	PL + 6ns	–	PL + 6ns	–	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	80	160	96	192	CK	
Time from alert asserted until DES commands required in persistent CA parity mode	tPAR_ALERT_RSP	–	64	–	71	–	85	CK	
CAL Timing									
CS_n to command address latency	tCAL	5	–	5	–	6	–	CK	20
CS_n to command address latency in gear-down mode	tCALg	N/A	–	6	–	8	–	CK	
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	MIN = tMOD (MIN) + tCPDED (MIN)						CK	1
Valid clock requirement after MPSM entry	tCKMPE	MIN = tMOD (MIN) + tCPDED (MIN)						CK	1

Parameter		Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
MPSM Timing										
Valid clock requirement before MPSM exit		tCKMPX	MIN = tCKSRX (MIN)						CK	1
Exit MPSM to commands not requiring a locked DLL		tXMP	tXS (MIN)						CK	
Exit MPSM to commands requiring a locked DLL		tXMPDLL	MIN = tXMP (MIN) + tXSDLL (MIN)						CK	1
CS setup time to CKE		tMPX_S	MIN = tIS (MIN) + tIH (MIN)						ns	
CS_n HIGH hold time to CKE rising edge		tMPX_HH	MIN = tXP						ns	
CS_n LOW hold time to CKE rising edge		tMPX_LH	12	tXMP-1 0ns	12	tXMP-1 0ns	12	tXMP-1 0ns	ns	
Connectivity Test Timing										
TEN pin HIGH to CS_n LOW – Enter CT mode		tCT_Enable	200	–	200	–	200	–	ns	
CS_n LOW and valid input to valid output		tCT_Valid	–	200	–	200	–	200	ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		tCTCKE_Valid	10	–	10	–	10	–	ns	
Calibration and VREFDQ Train Timing										
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	1024	–	1024	–	1024	–	CK	
	Normal operation	tZQoper	512	–	512	–	512	–	CK	
ZQCS command: Short calibration time		tZQCS	128	–	128	–	128	–	CK	
The VREF increment/decrement step time		VREF_time	MIN = 150ns							
Enter VREFDQ training mode to the first write or VREFDQ MRS command delay		tVREFDQE	MIN = 150ns						ns	1
Exit VREFDQ training mode to the first WRITE command delay		tVREFDQX	MIN = 150ns						ns	1

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Initialization and Reset Timing										
Exit reset from CKE HIGH to a valid command	tXPR	MIN = greater of 5CK or tRFC (MIN) + 10ns						CK	1	
RESET_L pulse low after power stable	tPW_REST_S	1.0	–	1.0	–	1.0	–	µs		
RESET_L pulse low at power-up	PW_REST_L	200	–	200	–	200	–	µs		
Begin power supply ramp to power supplies stable	tVDDPR	MIN = N/A; MAX = 200						ms		
RESET_n LOW to power supplies stable	tRPS	MIN = 0; MAX = 0						ns		
RESET_n LOW to I/O and RTT High-Z	tIOZ	MIN = N/A; MAX = undefined						ns		
Refresh Timing										
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	tRFC1	MIN = 260						ns	1, 12
		tRFC2	MIN = 160						ns	1, 12
		tRFC4	MIN = 110						ns	1, 12
	8Gb	tRFC1	MIN = 350						ns	1, 12
		tRFC2	MIN = 260						ns	1, 12
		tRFC4	MIN = 160						ns	1, 12
	16Gb	tRFC1	MIN = 550						ns	1, 12
		tRFC2	MIN = 350						ns	1, 12
		tRFC4	MIN = 260						ns	1, 12
Average periodic refresh interval	0°C ≤ TC ≤ 85°C	tREFI	MIN = N/A; MAX = 7.8						ns	12
	85°C < TC ≤ 95°C	tREFI	MIN = N/A; MAX = 3.9						µs	12
Self Refresh Timing										
Exit self refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self refresh abort	tXS	MIN = tRFC + 10ns						ns	1	
	tXS_ABORT	MIN = tRFC4 + 10ns						ns	1	
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)	tXS_FAST	MIN = tRFC4 + 10ns						ns	1	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Self Refresh Timing									
Exit self refresh to commands requiring a locked DLL	tXSDLL	MIN = tDLLK (MIN)						CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing	tCKESR	MIN = tCKE (MIN) + 1nCK						CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled	tCKESR_PAR	MIN = tCKE (MIN) + 1nCK + PL						CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)	tCKSRE	MIN = greater of (5CK, 10ns)						CK	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled	tCKSRE_PAR	MIN = greater of (5CK, 10ns) + PL						CK	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	tCKSRX	MIN = greater of (5CK, 10ns)						CK	1
Power-Down Timing									
Exit power-down with DLL on to any valid command	tXP	MIN = greater of 4CK or 6ns						CK	1
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled	tXP_PAR	MIN = (greater of 4CK or 6ns) + PL						CK	1
CKE MIN pulse width	tCKE (MIN)	MIN = greater of 3CK or 5ns						CK	
Command pass disable delay	tCPDED	4	-	4	-	4	-	CK	
Power-down entry to power-down exit timing	tPD	MIN = tCKE (MIN); MAX = 9 × tREFI						CK	
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK						CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time						CK	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Power-Down Timing									
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXSDLL						CK	
Power-Down Entry Minimum Timing									
ACTIVATE command to power-down entry	tACTPDEN	2	-	2	-	2	-	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	2	-	2	-	2	-	CK	
REFRESH command to power-down entry	tREFPDEN	2	-	2	-	2	-	CK	
MRS command to power-down entry	tMRSPDEN	MIN = tMOD (MIN)						CK	1
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1						CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	MIN = WL + 4 + tWR/tCK (AVG)						CK	1
WRITE command to power-down entry(BC4MRS)	tWRPBC4DEN	MIN = WL + 2 + tWR/tCK (AVG)						CK	1
WRITE with auto precharge command to power-down entry (BL8OTF,BL8MRS,BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1						CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1						CK	1
ODT Timing									
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2						CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2						CK	
R _{TT} dynamic change skew	tADC	0.3	0.7	0.28	0.72	0.26	0.74	CK	
Asynchronous R _{TT(NOM)} turn-on delay (DLL off)	tAONAS	1	9	1	9	1	9	ns	
Asynchronous R _{TT(NOM)} turn-off delay (DLL off)	tAOFAS	1	9	1	9	1	9	ns	

Parameter	Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
ODT Timing									
ODT HIGH time with WRITE command and BL8	ODTH8 1'CK	6	–	6	–	6	–	CK	
	ODTH8 2'CK	7	–	7	–	7	–		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1'CK	4	–	4	–	4	–	CK	
	ODTH4 2'CK	5	–	5	–	5	–		
Write Leveling Timing									
First DQS _t , DQS _c rising edge after write leveling mode is programmed	tWLMRD	40	–	40	–	40	–	CK	
DQS _t , DQS _c delay after write leveling mode is programmed	tWLDQSEN	25	–	25	–	25	–	CK	
Write leveling setup from rising CK _t , CK _c crossing to rising DQS _t , DQS _c crossing	tWLS	0.13	–	0.13	–	0.13	–	tCK (AVG)	
Write leveling hold from rising DQS _t , DQS _c crossing to rising CK _t , CK _c crossing	tWLH	0.13	–	0.13	–	0.13	–	tCK (AVG)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	
Gear-Down Timing (Not Supported Below DDR4-2666)									
Exit reset from CKE HIGH to a valid MRS gear-down	tXPR_GEAR	N/A		tXPR		tXPR		CK	
CKE HIGH assert to gear-down enable time	tXS_GEAR	N/A		tXS		tXS		CK	
MRS command to sync pulse time	tSYNC_GEAR	N/A		tMOD + 4CK tMOD		tMOD + 4CK tMOD		CK	
Sync pulse to first valid command	tCMD_GEAR	N/A		tMOD		tMOD		CK	
Gear-down setup time	tGEAR_setup	N/A	–	2CK	–	2CK	–	CK	
Gear-down hold time	tGEAR_hold	N/A	–	2CK	–	2CK	–	CK	

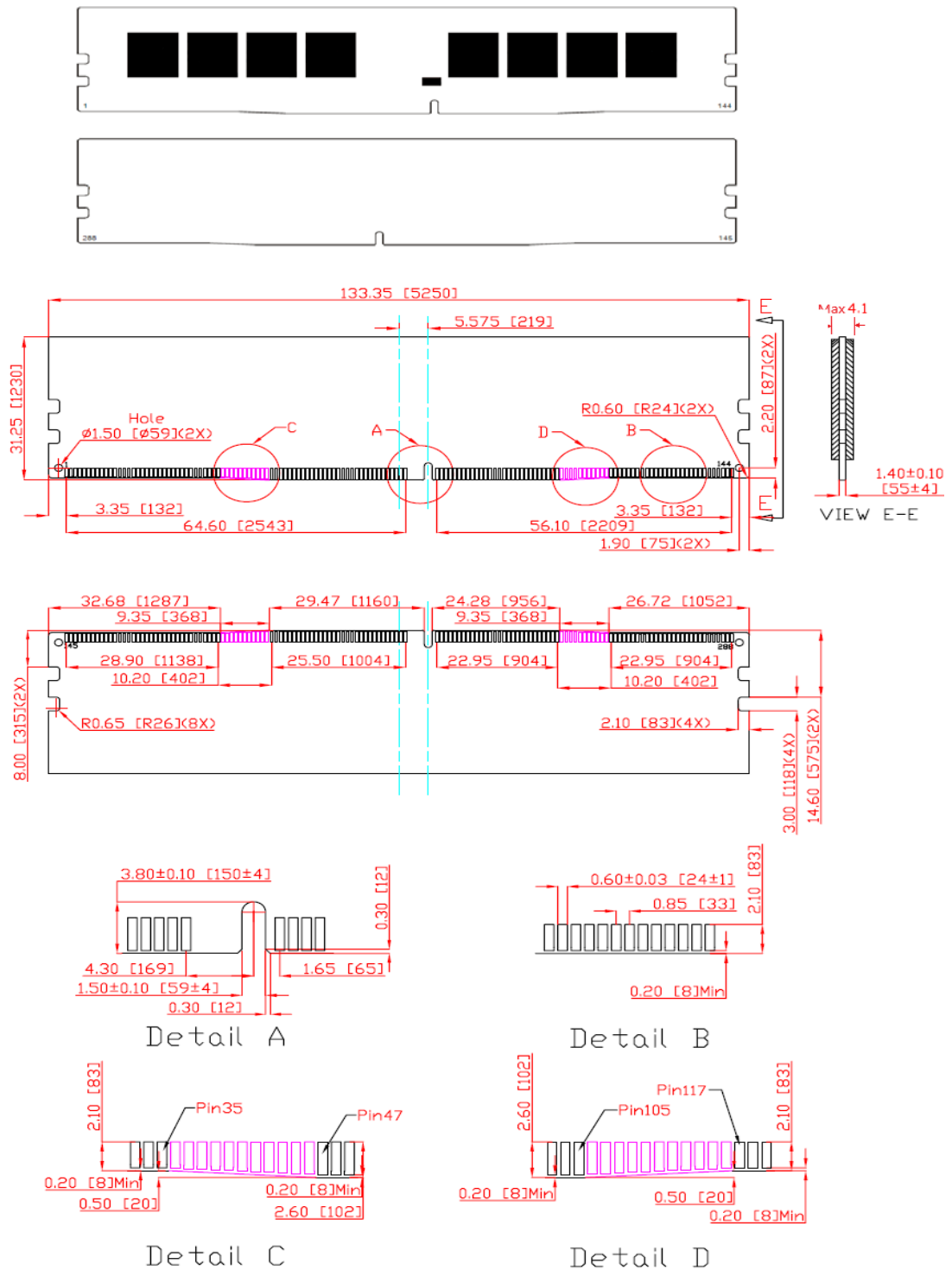
Notes:

- (1) Maximum limit not applicable.
- (2) tCCD_L and tDLLK should be programmed according to the value defined per operating frequency.
- (3) Data rate is greater than or equal to 1066 Mb/s.
- (4) RFU.
- (5) WRITE-to-READ when CRC and DM are both not enabled.
- (6) WRITE-to-READ delay when CRC and DM are both enabled.
- (7) The start of internal write transactions is defined as follows:
 - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
 - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
- (8) For these parameters, the device supports $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns]/t_{CK} (AVG) [ns]\}$, in clock cycles, assuming all input clock jitter specifications are satisfied.
- (9) Although unlimited row accesses to the same row is allowed within the refresh period, excessive row accesses to the same row over a long term can result in degraded operation.
- (10) When operating in 1tCK WRITE preamble mode.
- (11) When operating in 2tCK WRITE preamble mode.
- (12) When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to tRFC refresh time.
- (13) DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
- (14) Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.
- (15) JEDEC specifies a minimum of five clocks.
- (16) The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZ(DQS) MAX on the right side.
- (17) The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately $0.7 \times V_{DDQ}$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $V_{TT} = V_{DDQ}$.
- (18) JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
- (19) Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
- (20) The actual tCAL minimum is the larger of 3 clocks or 3.748ns/tCK; the table lists the applicable clocks required at targeted speed bin.
- (21) The maximum READ preamble is bounded by tLZ(DQS) MIN on the left side and tDQSCK (MAX) on the right side. See figure in Clock to Data Strobe Relationship. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in READ Preamble.

- (22) DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
- (23) The tPDA_S/tPDA_H parameters may use the tDS/tDH limits, respectively, if the signal is LOW the entire BL8.

Package Dimensions :

[8GB – 1Rank, 1024Mx8 DDR4 SDRAMs]



Note: All dimensions are in millimeters(mils) and should be kept within a tolerance of ± 0.15 (5.91), unless otherwise specified.